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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,715	06/26/2003	Benjamin Thomas Percer	200312936-1	5780

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EXAMINER	
LE, JOHN H	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,715	PERCER ET AL.	
	Examiner	Art Unit	
	John H. Le	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,13-28 and 30-32* is/are rejected.

7)☒ Claim(s) *9-12 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *26 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/27/2005 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-8, 13, 16, 22, 24-27, 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushige (US 2003/0101020 A1) in view of Cully et al. (USP 6,000,040) and Iswandhi et al. (USP 5,675,807).

Regarding claims 1, 24, and 31, Matsushige discloses a system for margin testing one or more components of an electronic system (Abstract), comprising a fault bypass module (port bypass circuit) incorporated in said electronic system, said fault bypass module configured to indicate of one or more faults associated with one or more of said components during margin testing of said electronic system ([0143]-[0145]).

Regarding claim 22, Matsushige discloses a system for margin testing one or more components of the electronic system (Abstract), comprising: a fault bypass module (port bypass circuit) incorporated in said electronic system, said fault bypass module configured to indicate of one or more faults associated with one or more of said components during margin testing of said electronic system ([0143]-[0145]), and an internal controller (15) in communication with said fault bypass module, said internal controller configured to transmi a command to said fault bypass module to initiate masking of said fault signals by said module ([0055]-[0057], [0062]).

Matsushige fails to teach the fault bypass module to intercept at least one signal indicative of one or more faults associated with one or more of said components and mask the at least one signal indicative of one or more fault by generating at least one signal indicative of absence of the one or more faults.

Cully et al. teach the fault bypass module (programmable fault detector) to intercept (interrupt) at least one signal indicative of one or more faults associated with one or more of said components and mask the at least one signal indicative of one or more fault (e.g. Col.1, line 52-Col.2, line 18, Col.8, lines 10-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a fault bypass module to intercept at least one signal indicative of one or more faults associated with one or more of said components and mask the at least one signal indicative of one or more fault as taught by Cully et al. in a margin test method of Matsushige for the purpose of providing an apparatus and

method for managing faults in a computer system having circuits (Cully et al., Col.1, lines 42-50).

Iswandhi et al. teach the fault bypass module (mask check 177) mask the at least one signal indicative of one or more fault (e.g. Col.32, lines 45-53) by generating at least one signal indicative of absence of the one or more faults (Col.2, line67-Col.3, line 6).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a fault bypass module to mask the at least one signal indicative of one or more fault by generating at least one signal indicative of absence of the one or more faults as taught by Iswandhi et al. in a margin test method of Matsushige in view of Cully et al. for the purpose of providing a fault-tolerant operation through both "fail-fast" and "fail-functional" operation. Fail-fast operation is achieved by locating error-checking capability at strategic points of the system (Iswandhi et al., Col.5, lines 8-12).

Regarding claim 2, Matsushige discloses at least one of said one or more faults corresponds to an operating parameter associated with at least one of said one or more components crossing a selected threshold ([0057]-[0061], [0128]).

Regarding claim 3, Matsushige discloses said operating parameter is any of voltage ([0066]).

Regarding claim 4, Matsushige discloses a controller (15) incorporated in said electronic system and in communication with said fault bypass module, said controller

configured to transmit a command to said fault bypass module to initiate masking of said fault signals by said module ([0055]-[0057], [0062]).

Regarding claim 6, Matsushige discloses said fault bypass module permits normal processing of said fault signals during normal operation of said electronic system ([0100]).

Regarding claim 7, Matsushige discloses a hardware monitor (micro processor 15) configured to communication with said controller and with at least one of said one or more components, and to generate a fault signal in response to an occurrence of a fault associated with said at least one component ([0088]-[0091]).

Regarding claim 8, Matsushige discloses said hardware monitor is further configured to transmit said fault signal to said fault bypass module, and wherein said fault bypass module is further configured to mask said received fault signal during margin testing of said electronic device ([0088]).

Regarding claim 13, Matsushige discloses a programmable logic device programmed to provide masking of said fault signals (0141]).

Regarding claim 16, Matsushige discloses said electronic system comprises a computer system ([0066]).

Regarding claims 25-28, Matsushige discloses a power control element in absence of margin testing, supplying to said power control element a signal indicative of absence of a fault indicated by said fault signals, a voltage associated with a power rail varying from a nominal value by more than a selected threshold , reducing power applied to said power rail (e.g. [0055]-[0068], [0100]-[0113]).

Regarding claim 30, Matsushige discloses said electronic system is a computer server ([0066]).

Regarding claim 5, Cully et al. teach said fault signals comprise: one or more interrupt signals (e.g. Col.1, line 52-Col.2, line 18, Col.8, lines 10-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a fault bypass module to mask the at least one signal indicative of one or more fault by generating at least one signal indicative of absence of the one or more faults as taught by Iswandhi et al. in a margin test method of Matsushige in view of Cully et al. for the purpose of providing a fault-tolerant operation through both "fail-fast" and "fail-functional" operation. Fail-fast operation is achieved by locating error-checking capability at strategic points of the system (Iswandhi et al., Col.5, lines 8-12).

4. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushige (US 2003/0101020 A1) in view of Cully et al. (USP 6,000,040).

Regarding claim 32, Matsushige discloses a system for margin testing one or more components of the electronic system (Abstract), comprising: a fault bypass module (port bypass circuit) incorporated in said electronic system, said fault bypass module configured to indicate of one or more faults associated with one or more of said components during margin testing of said electronic system ([0143]-[0145]).

Matsushige fails to teach a fault bypass module incorporated in said computer server, said fault bypass module configured to mask signals indicative of one or more faults associated with one or more of said components.

Cully et al. teach a fault bypass module (programmable fault detector) incorporated in said computer server, said fault bypass module configured to mask signals indicative of one or more faults associated with one or more of said components (e.g. Col.1, line 52-Col.2, line 18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a fault bypass module incorporated in said computer server, said fault bypass module configured to mask signals indicative of one or more faults associated with one or more of said components as taught by Cully et al. in a margin test method of Matsushige for the purpose of providing an apparatus and method for managing faults in a computer system having circuits (Cully et al., Col.1, lines 42-50).

5. Claim 18-21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushige (US 2003/0101020 A1) in view of Cully et al. (USP 6,000,040) and Iswandhi et al. (USP 5,675,807) as applied to claim 1 above, and further in view of Hawkins et al. (US 2003/0130969 A1).

Regarding claims 18-21 and 23, Matsushige, Cully et al., and Iswandhi et al. fail to disclose a controller comprises a Baseboard Management Controller (BMC), wherein said communication bus is an Inter-Integrated Circuit bus (I^2C bus), wherein said I^2C bus is Intelligent Platform Management Bus (IPMB).

Hawkins et al. disclose a controller comprises a Baseboard Management Controller (BMC) ([0015]-[0017]), wherein said communication bus is an Inter-Integrated Circuit bus (I^2C bus)([0006]), wherein said I^2C bus is IPMB ([0013]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a Baseboard Management Controller (BMC), an Inter-Integrated Circuit bus (I^2C bus), wherein said I^2C bus is Intelligent Platform Management Bus (IPMB) as taught by Hawkins et al. in a margin test method of Matsushige in view of Cully et al. and Iswandhi et al. for the purpose of providing a star Intelligent Platform Management Bus Topology.

Allowable Subject Matter

6. Claims 9-12, 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 9, none of the prior art of record teaches or suggests the combination of a margin testing system for margin testing one or more components of the computer system, comprising: a fault bypass module incorporated in said electronic system, said fault bypass module configured to intercept at least one signal and masking signals indicative of one or more faults associated with one or more of said components during margin testing of said electronic system and mask the at least one signal indicative of one or more fault by generating at least one signal indicative of absence of the one or more faults; and a power control element in communication with said fault bypass module, said fault bypass module transmitting one of more of said fault signals to said power control element in absence of margin testing and masking

said one or more fault signals during margin testing of said electronic system. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 11, none of the prior art of record teaches or suggests the combination of a margin testing system for margin testing one or more components of the computer system, comprising: a fault bypass module incorporated in said electronic system, said fault bypass module configured to intercept at least one signal and masking signals indicative of one or more faults associated with one or more of said components during margin testing of said electronic system and mask the at least one signal indicative of one or more fault by generating at least one signal indicative of absence of the one or more faults; a controller internal to said electronic system and in communication with said fault bypass module, said controller transmitting a command to said fault bypass module for initiating masking of said fault signals by said module; and a hardware monitor in communication with said controller and with at least one of said components, said hardware generating an fault signal in response to occurrence of a fault associated with said at least one component; wherein said at least one component is a power rail, and said hardware monitor generates an interrupt signal in response to a voltage associated with said power rail varying from a nominal value by more than a selected threshold. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 29, none of the prior art of record teaches or suggests the combination of a method of masking faults during margin testing of an electronic system, wherein the method comprising: intercepting one or more signals indicative of faults associated with one or more components of said electronic system during margin testing thereof; and generating at least one signal indicative of absence of said fault; thereby masking said intercepted signals, wherein intercepting one or more signals, comprises: intercepting a selected output signal of said one or more components; and wherein generating signals indicative of absence of said faults, comprises: generating a simulated signal corresponding to said intercepted output signal for transmittal to a hardware monitor. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Response to Arguments

7. Applicant's arguments filed 12/27/2005 have been fully considered but they are not persuasive.

-Applicant argues that the prior did not teach, "generating at least one signal indicative of absence of said fault; thereby masking said intercepted signals" as citied in claims 1, 22, 24, and 31.

Examiner position is that the prior did teach, "generating at least one signal indicative of absence of said fault; thereby masking said intercepted signals" as discussed above.

-Applicant argues that the prior did not teach, "a fault bypass module incorporated in a computer server" as citied in claim 32.

Examiner position is that the prior did teach, "a fault bypass module incorporated in a computer server" as discussed above.

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John H. Le whose telephone number is 571 272 2275. The examiner can normally be reached on 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Barlow can be reached on 571 272 2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John H. Le

Patent Examiner-Group 2863

March 17, 2006

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